APPENDIX

Claims on Appeal

1. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

2. The dynamic logic circuit of claim 1 wherein said precharge circuit comprises a PMOS transistor.

3. The dynamic logic circuit of claim 1 wherein said ground switch circuit comprises a NMOS transistor.

5. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

6. The dynamic logic circuit of claim 5 wherein said precharge circuit comprises a PMOS transistor.

7. The dynamic logic circuit of claim 5 wherein said ground switch circuit comprises a NMOS transistor.

9. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node which is connected to said first common node of said pull-down network.

10. The dynamic logic circuit of claim 9 wherein said precharge circuit comprises a PMOS transistor.

11. The dynamic logic circuit of claim 9 wherein said ground switch circuit comprises a NMOS transistor.

13. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node connected to said first common node of said pull-down network.

14. The dynamic logic circuit of claim 13 wherein said precharge circuit comprises a PMOS transistor.

15. The dynamic logic circuit of claim 13 wherein said ground switch circuit comprises a NMOS transistor.